# XCR3064XL 64 Macrocell CPLD

DS017 (v1.0) June 1, 2000

**Preliminary Product Specification**

## Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to 145 MHz
- 64 macrocells with 1,500 usable gates
- Available in small footprint packages
  - 100-pin TQFP (64 user I/O pins)
  - 44-pin VQFP (32 user I/O)
  - 56-ball CP BGA (44 user I/O)
- Optimized for 3.3V systems
  - Ultra-low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer reprogrammable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

## Description

The XCR3064XL is a 3.3V, 64-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four logic blocks provide 1,500 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz.

## TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the $I_{CC}$ vs. Frequency of our XCR3064XL TotalCMOS CPLD (data taken with four up/down, loadable 16-bit counters at 3.3V, 25°C).

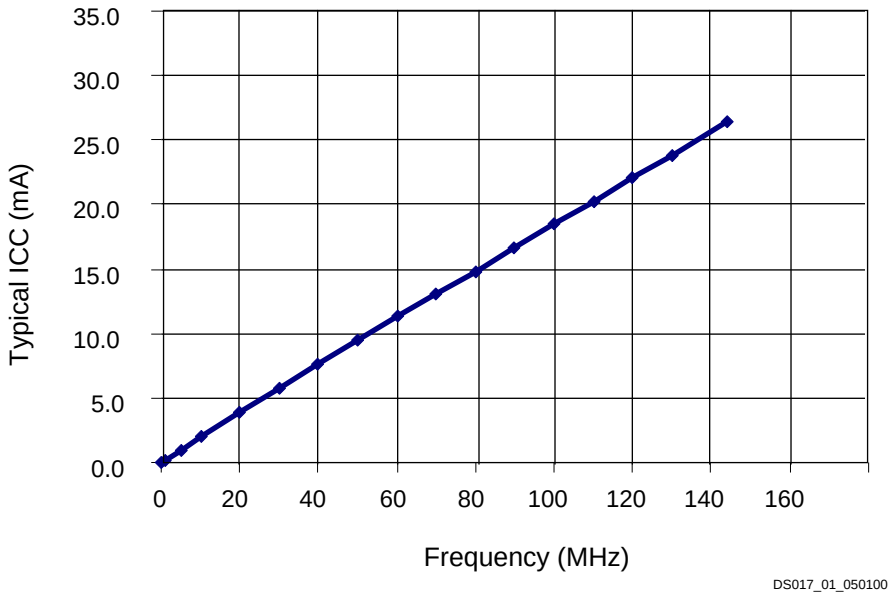



*Figure 1:* **$I_{CC}$ vs. Frequency at $V_{CC}$ = 3.3V, 25°C**

*Table 1:* **$I_{CC}$ vs. Frequency** ($V_{CC}$ = 3.3V, 25°C)

| Frequency (MHz) | 0 | 1 | 5 | 10 | 20 | 40 | 60 | 80 | 100 | 120 | 140 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Typical $I_{CC}$ (mA) | 0 | 0.2 | 1.0 | 2.0 | 3.9 | 7.6 | 11.3 | 14.8 | 18.5 | 22.1 | 25.6 |

## DC Electrical Characteristics Over Recommended Operating Conditions(1)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High voltage for 3.3V outputs | $I_{OH}$ = –8 mA | 2.4 | - | V |
| $V_{OL}$ | Output Low voltage for 3.3V outputs | $I_{OL}$ = 8 mA | - | 0.4 | V |
| $I_{IL}$ | Input leakage current | $V_{IN}$ = GND or $V_{CC}$ | –10 | 10 | µA |
| $I_{IH}$ | I/O High-Z leakage current | $V_{IN}$ = GND or $V_{CC}$ | –10 | 10 | µA |
| $I_{CCSB}$ | Standby current | $V_{CC}$ = 3.6V | - | 100 | µA |
| $I_{CC}$ | Dynamic current(2,3) | f = 1 MHz | - | 0.5 | mA |
| | | f = 50 MHz | - | 15 | mA |
| $C_{IN}$ | Input pin capacitance(4) | f = 1 MHz | - | 8 | pF |
| $C_{CLK}$ | Clock input capacitance(4) | f = 1 MHz | - | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance(4) | f = 1 MHz | - | 10 | pF |

**Notes:**
1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See Table 1, Figure1 for typical values.
3. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to $V_{CC}$ or ground. This parameter guaranteed by design and characterization, not testing.
4. Typical values not tested.

# AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

| Symbol | Parameter | -6 | | -7 | | -10 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $T_{PD1}$ | Propagation delay time (single p-term) | - | 5.5 | - | 7.0 | - | 9.1 | ns |
| $T_{PD2}$ | Propagation delay time (OR array)(3) | - | 6.0 | - | 7.5 | - | 10.0 | ns |
| $T_{CO}$ | Clock to output (global synchronous pin clock) | - | 4.0 | | 5.0 | - | 6.5 | ns |
| $T_{SUF}$ | Setup time fast | 2.0 | - | 2.5 | - | 3.0 | - | ns |
| $T_{SU}$ | Setup time | 4.0 | - | 4.8 | - | 6.3 | - | ns |
| $T_{H}$ | Hold time | 0 | - | 0 | - | 0 | - | ns |
| $T_{WLH}$ | Global Clock pulse width (High or Low) | 2.5 | - | 3.0 | - | 4.0 | - | ns |
| $Tt_{PLH}$ | P-term clock pulse width | 4.0 | - | 5.0 | - | 6.0 | - | ns |
| $T_{R}$ | Input rise time | - | 20 | - | 20 | - | 20 | ns |
| $T_{L}$ | Input fall time | - | 20 | - | 20 | - | 20 | ns |
| $f_{SYSTEM}$ | Maximum system frequency | - | 145 | - | 119 | - | 95 | MHz |
| $T_{CONFIG}$ | Configuration time(4) | - | 20.0 | - | 20.0 | - | 20.0 | µs |
| $T_{POE}$ | P-term OE to output enabled | - | 7.5 | - | 9.3 | - | 11.2 | ns |
| $T_{POD}$ | P-term OE to output disabled(5) | - | 7.5 | - | 9.3 | - | 11.2 | ns |
| $T_{PCO}$ | P-term clock to output | - | 6.5 | - | 8.3 | - | 10.7 | ns |
| $T_{PAO}$ | P-term set/reset to output valid | - | 8.0 | - | 9.3 | - | 11.2 | ns |

**Notes:**
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 4 for derating.
4. Typical current draw during configuration is 8 mA at 3.6V.
5. Output $C_L$ = 5 pF.

## Timing Model

The XPLA3 architecture follows a simple timing model that allows deterministic timing in design and redesign. The basic timing model is shown in Figure 2. One key feature of the XPLA3 CPLD is the ability to have up to 48 product term inputs into a single macrocell and maintain consistent timing. This is achieved through the use of a fully populated PLA (Programmable AND Programmable OR Array) which also has the ability to share product terms and only use the required amount of product terms per macrocell. There is a fast path ($T_{LOGI1}$) into the macrocell which is used if there is a single product term. The $T_{LOGI2}$ path is used for multiple product term timing. For optimization of logic, the XPLA3 CPLD architecture includes a Fold-back NAND path ($T_{LOGI3}$). There is a fast input path to each macrocell if used as an Input Register ($T_{FIN}$). XPLA3 also includes universal control terms ($T_{UDA}$) that can be used for synchronization of the macrocell registers in different logic blocks. There is also slew rate control and output enable control on a per macrocell basis.

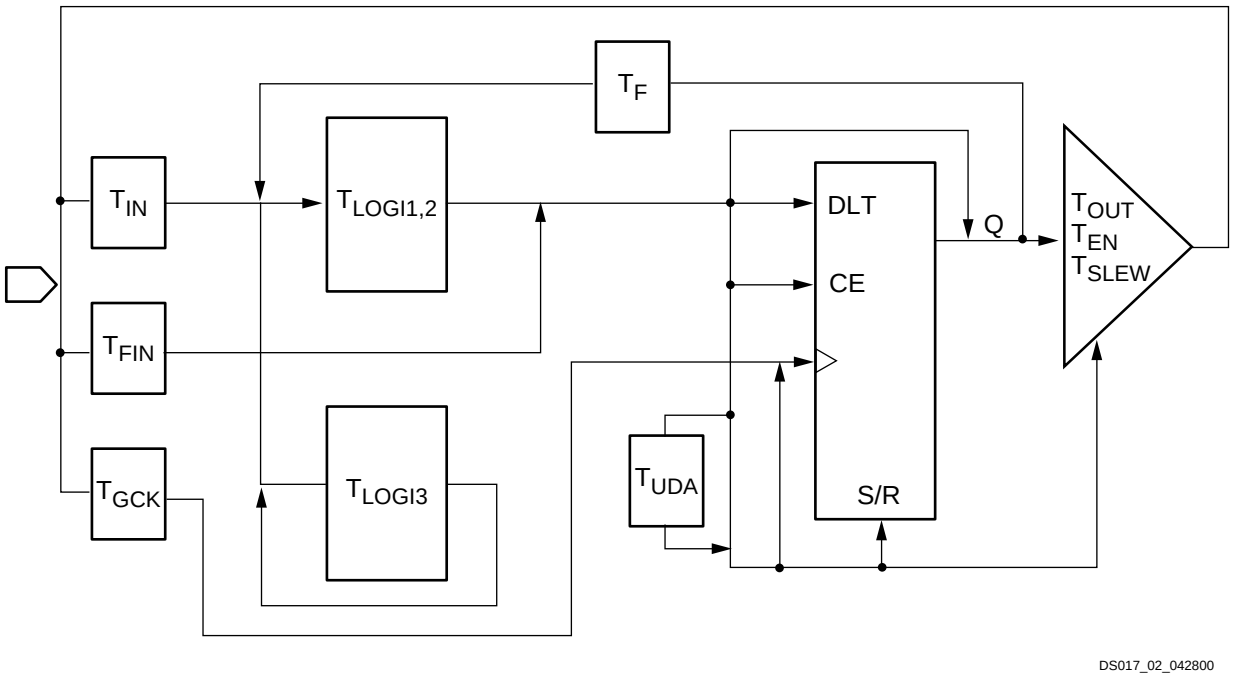
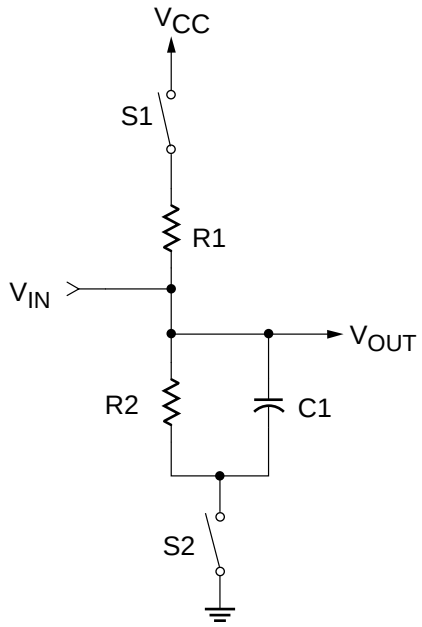



*Figure 2:* **XPLA3 Timing Model**

# Internal Timing Parameters

| Symbol | Parameter | -6 | | -7 | | -10 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Buffer Delays** | | | | | | | | |
| $T_{IN}$ | Input buffer delay | - | 1.3 | - | 1.6 | - | 2.2 | ns |
| $T_{FIN}$ | Fast Input buffer delay | - | 1.8 | - | 2.5 | - | 3.1 | ns |
| $T_{GCK}$ | Global Clock buffer delay | - | 0.8 | - | 1.0 | - | 1.3 | ns |
| $T_{OUT}$ | Output buffer delay | - | 2.2 | - | 2.7 | - | 3.6 | ns |
| $T_{EN}$ | Output buffer enable/disable delay | - | 4.2 | - | 5.0 | - | 5.7 | ns |
| **Internal Register and Combinatorial Delays** | | | | | | | | |
| $T_{LDI}$ | Latch transparent delay | - | 1.3 | - | 1.6 | - | 2.0 | |
| $T_{SUI}$ | Register setup time | 1.0 | - | 1.0 | - | 1.2 | - | ns |
| $T_{HI}$ | Register hold time | 4.0 | - | 5.5 | - | 6.7 | - | ns |
| $T_{ECSU}$ | Register clock enable setup time | 2.0 | - | 2.5 | - | 3.0 | - | ns |
| $T_{ECHO}$ | Register clock enable hold time | 3.0 | - | 4.5 | - | 5.5 | - | ns |
| $T_{COI}$ | Register clock to output delay | - | 1.0 | - | 1.3 | - | 1.6 | ns |
| $T_{AOI}$ | Register async. S/R to output delay | - | 2.5 | - | 2.3 | - | 2.1 | ns |
| $T_{RAI}$ | Register async. recovery | - | 4.0 | - | 5.0 | - | 6.0 | ns |
| $T_{LOGI1}$ | Internal logic delay (single p-term) | - | 2.0 | - | 2.7 | - | 3.3 | ns |
| $T_{LOGI2}$ | Internal logic delay (PLA OR term) | - | 2.5 | - | 3.2 | - | 4.2 | ns |
| **Feedback Delays** | | | | | | | | |
| $T_F$ | ZIA delay | - | 2.4 | - | 2.9 | - | 3.5 | ns |
| **Time Adders** | | | | | | | | |
| $T_{LOGI3}$ | Fold-back NAND delay | - | 6.0 | - | 7.5 | - | 9.5 | ns |
| $T_{UDA}$ | Universal delay | - | 1.5 | - | 2.0 | - | 2.5 | ns |
| $T_{SLEW}$ | Slew rate limited delay | - | 4.0 | - | 5.0 | - | 6.0 | ns |

## Switching Characteristics




| Component | Values |
|---|---|
| R1 | 390Ω |
| R2 | 390Ω |
| C1 | 35 pF |

| Measurement | S1 | S2 |
|---|---|---|
| $T_{POE}$ (High) | Open | Closed |
| $T_{POE}$ (Low) | Closed | Open |
| $T_P$ | Closed | Closed |

**Note:** For $T_{POD}$, C1 = 5 pF

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*Figure 3:* **AC Load Circuit**

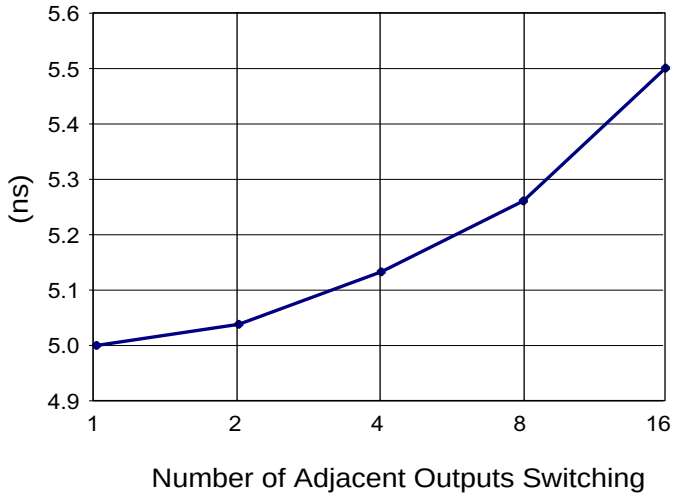


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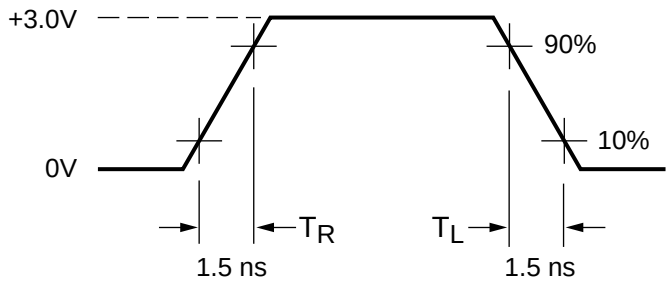
*Figure 4:* **Derating Curve for $T_{PD2}$**




**Measurements:**
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

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*Figure 5:* **Voltage Waveform**

# Pin Descriptions

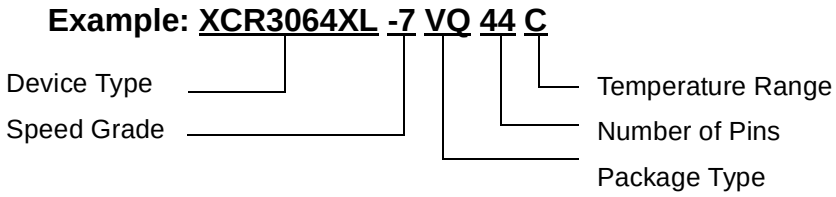
*Table 2:* **XCR3064XL Pin Descriptions**

| Function | 100VQFP | 44VQFP | CP56 | BScan Order |
|---|---|---|---|---|
| A0 | 85 | 35 | C8 | 256 |
| A1 | 84 | 34 | A8 | 252 |
| A2 | 83 | - | - | 248 |
| A3 | 81 | - | A9 | 244 |
| A4 | 80 | - | A5 | 240 |
| A5 | 79 | - | A10 | 236 |
| A6 | 76 | - | - | 232 |
| A7 | 75 | 33 | B10 | 228 |
| A8/TDO | 73 (TDO) | 32 (TDO) | C10 (TDO) | - |
| A9 | 71 | 31 | D8 | 220 |
| A10 | 69 | 30 | E8 | 216 |
| A11 | 68 | - | - | 212 |
| A12 | 67 | - | - | 208 |
| A13 | 65 | 28 | F8 | 204 |
| A14 | 64 | 27 | E10 | 200 |
| A15 | 63 | - | - | 196 |
| B0 | 92 | 42 | C4 | 128 |
| B1 | 93 | 43 | C3 | 124 |
| B2 | 94 | 44 | A1 | 120 |
| B3 | 96 | - | - | 116 |
| B4 | 97 | - | B1 | 112 |
| B5 | 98 | - | - | 108 |
| B6 | 99 | - | A2 | 104 |
| B7 | 100 | - | A3 | 100 |
| B8/TDI | 4 (TDI) | 1 (TDI) | C1 (TDI) | - |
| B9 | 6 | 2 | D1 | 92 |
| B10 | 8 | 3 | D3 | 88 |
| B11 | 9 | - | - | 84 |
| B12 | 10 | - | - | 80 |
| B13 | 12 | 5 | E3 | 76 |
| B14 | 13 | 6 | F1 | 72 |
| B15 | 14 | - | - | 68 |
| C0/TCK | 62 (TCK) | 26 (TCK) | F10 (TCK) | - |
| C1 | 61 | 25 | G8 | 188 |
| C2 | 60 | - | - | 184 |
| C3 | 58 | 23 | H10 | 180 |
| C4 | 57 | - | - | 176 |
| C5 | 56 | - | - | 172 |
| C6 | 54 | - | K8 | 168 |
| C7 | 52 | - | K10 | 164 |
| C8 | 48 | 22 | K9 | 160 |
| C9 | 47 | 21 | J10 | 156 |

*Table 2:* **XCR3064XL Pin Descriptions *(Continued)***

| Function | 100VQFP | 44VQFP | CP56 | BScan Order |
|---|---|---|---|---|
| C10 | 46 | 20 | H8 | 152 |
| C11 | 45 | 19 | H7 | 148 |
| C12 | 44 | 18 | H6 | 144 |
| C13 | 42 | - | - | 140 |
| C14 | 41 | - | K7 | 136 |
| C15 | 40 | - | - | 132 |
| CLK0/IN0 | 90 | 40 | C5 | 3 |
| CLK1/IN1 | 89 | 39 | C6 | 2 |
| CLK2/IN2 | 88 | 38 | C7 | 1 |
| CLK3/IN3 | 87 | 37 | A6 | 0 |
| D0/TMS | 15 (TMS) | 7 (TMS) | G1 (TMS) | - |
| D1 | 16 | 8 | F3 | 60 |
| D2 | 17 | - | - | 56 |
| D3 | 19 | 10 | G3 | 52 |
| D4 | 20 | 11 | J1 | 48 |
| D5 | 21 | - | - | 44 |
| D6 | 23 | - | - | 40 |
| D7 | 25 | - | K1 | 36 |
| D8 | 29 | 12 | K4 | 32 |
| D9 | 30 | 13 | K2 | 28 |
| D10 | 31 | 14 | K3 | 24 |
| D11 | 32 | 15 | H3 | 20 |
| D12 | 33 | - | H4 | 16 |
| D13 | 35 | - | - | 12 |
| D14 | 36 | - | K5 | 8 |
| D15 | 37 | - | - | 4 |
| PORT_EN | 11 (PE) | 4 (PE) | E1 (PE) | - |
| GND | 26 | - | - | - |
| GND | 38 | 16 | K6 | - |
| GND | 43 | - | - | - |
| GND | 59 | 24 | G10 | - |
| GND | 74 | - | - | - |
| GND | 86 | 36 | A7 | - |
| GND | 95 | - | - | - |
| $V_{CC}$ | 82 | - | - | - |
| $V_{CC}$ | 3 | - | - | - |
| $V_{CC}$ | 18 | 9 | H1 | - |
| $V_{CC}$ | 34 | - | - | - |
| $V_{CC}$ | 39 | 17 | H5 | - |
| $V_{CC}$ | 51 | - | - | - |
| $V_{CC}$ | 66 | 29 | D10 | - |
| $V_{CC}$ | 91 | 41 | A4 | - |

## Ordering Information




**Speed Options**

-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay
-6: 6.0 ns pin-to-pin delay

**Temperature Range**

C = Commercial $T_A$ = 0°C to +70°C
I = Industrial $T_A$ = –40°C to +85°C

**Packaging Options**

VQ100: 100-pin Very Thin Quad Flat Package
VQ44: 44-pin Very Thin Quad Flat Package
CP56: 56-ball Chip Scale Package

*Table 3:* **XCR3064XL JTAG Pinout by Package Type**

| Device XCR3064XL | (Pin Number) | | | | |
|---|---|---|---|---|---|
| | TCK | Port Enable | TMS | TDI | TDO |
| 100-pin TQFP | 62 | 11 | 15 | 4 | 73 |
| 44-pin VQFP | 26 | 4 | 7 | 1 | 32 |
| 56-ball CP BGA | F10 | E1 | G1 | C1 | C10 |

## Component Availability

| Pins | | 100 | 56 | 44 |
|---|---|---|---|---|
| Type | | Plastic VQFP | Plastic BGA | Plastic VQFP |
| Code | | TQ100 | CP56 | VQ44 |
| XCR3064XL | -6 | C | C | C |
| | -7, -10 | C,I | C,I | C,I |

## Revision History

The following table shows the revision history for this document..

| Date | Version | Revision |
|---|---|---|
| 06/01/00 | 1.0 | Initial Xilinx release. |
| | | |