XCR3128XL 128 Macrocell CPLD

DS016 (v1.1) May 3, 2000 **Preliminary Product Specification**

Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to 145 MHz
- 128 macrocells with 3,000 usable gates
- Available in small footprint packages
  - 144-pin TQFP (104 user I/O pins)
  - 144-ball CS BGA (104 user I/O)
  - 100-pin VQFP (80 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer reprogrammable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial temperature range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

Description

The XCR3128XL is a 3.3V 128 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of eight logic blocks provide 3,000 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3128XL TotalCMOS CPLD (data taken with eight up/down, loadable 16-bit counters at 3.3V, 25°C).

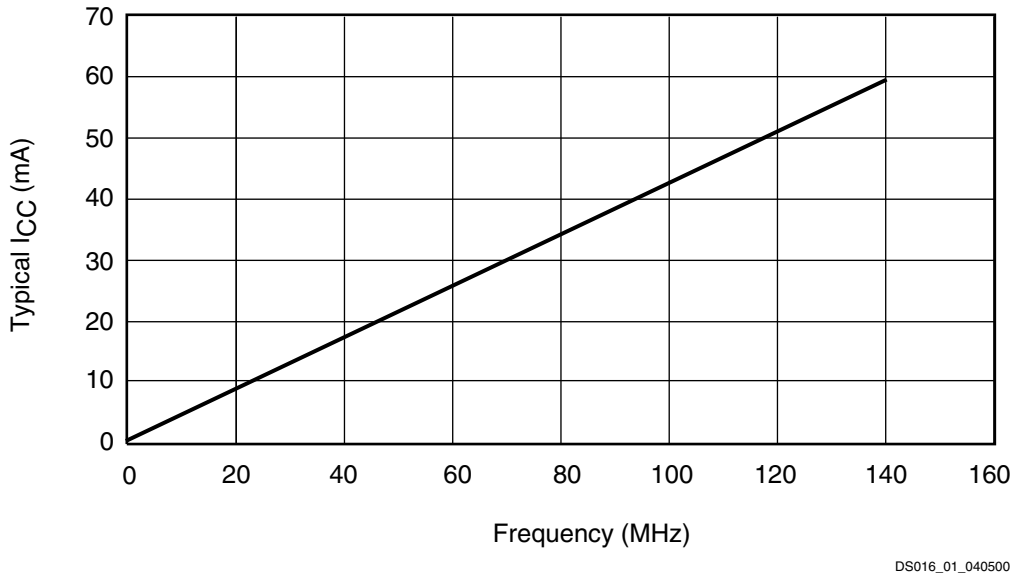


Figure 1: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0	0.5	2.2	4.4	8.7	17.1	25.3	33.6	41.6	49.7	57.7

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output High voltage for 3.3V outputs	I_{OH} = –8 mA	2.4	-	V
V_{OL}	Output Low voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(2,3)	f = 1 MHz	-	1	mA
		f = 50 MHz	-	30	mA
C_{IN}	Input pin capacitance(4)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(4)	f = 1 MHz	-	12	pF
$C_{I/O}$	I/O pin capacitance(4)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See Table 1, Figure1 for typical values.
3. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
4. Typical values not tested.

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	5.5	-	7.0	-	9.1	ns
T_{PD2}	Propagation delay time (OR array)(3)	-	6.0	-	7.5	-	10.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.0		5.0	-	6.5	ns
T_{SUF}	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T_{SU}	Setup time	4.0	-	4.8	-	6.3	-	ns
T_{H}	Hold time	0	-	0	-	0	-	ns
T_{WLH}	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
Tt_{PLH}	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T_{R}	Input rise time	-	20.0	-	20.0	-	20.0	ns
T_{L}	Input fall time	-	20.0	-	20.0	-	20.0	ns
f_{SYSTEM}	Maximum system frequency	-	145	-	119	-	95	MHz
T_{CONFIG}	Configuration time(4)	-	20.0	-	20.0	-	20.0	µs
T_{POE}	P-term OE to output enabled	-	7.5	-	9.3	-	11.2	ns
T_{POD}	P-term OE to output disabled(5)	-	7.5	-	9.3	-	11.2	ns
T_{PCO}	P-term clock to output	-	6.5	-	8.3	-	10.7	ns
T_{PAO}	P-term set/reset to output valid	-	8.0	-	9.3	-	11.2	ns
		Advance		**Preliminary**				

Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 4 for derating.
4. Typical current draw during configuration is 9 mA at 3.6V.
5. Output C_L = 5 pF.

Timing Model

The XPLA3 architecture follows a simple timing model that allows deterministic timing in design and redesign. The basic timing model is shown in Figure 2. One key feature of the XPLA3 CPLD is the ability to have up to 48 product term inputs into a single macrocell and maintain consistent timing. This is achieved through the use of a fully populated PLA (Programmable AND Programmable OR Array) which also has the ability to share product terms and only use the required amount of product terms per macrocell. There is a fast path (T_{LOGI1}) into the macrocell which is used if there is a single product term. The T_{LOGI2} path is used for multiple product term timing. For optimization of logic, the XPLA3 CPLD architecture includes a Fold-back NAND path (T_{LOGI3}). There is a fast input path to each macrocell if used as an Input Register (T_{FIN}). XPLA3 also includes universal control terms (T_{UDA}) that can be used for synchronization of the macrocell registers in different logic blocks. There is also slew rate control and output enable control on a per macrocell basis.

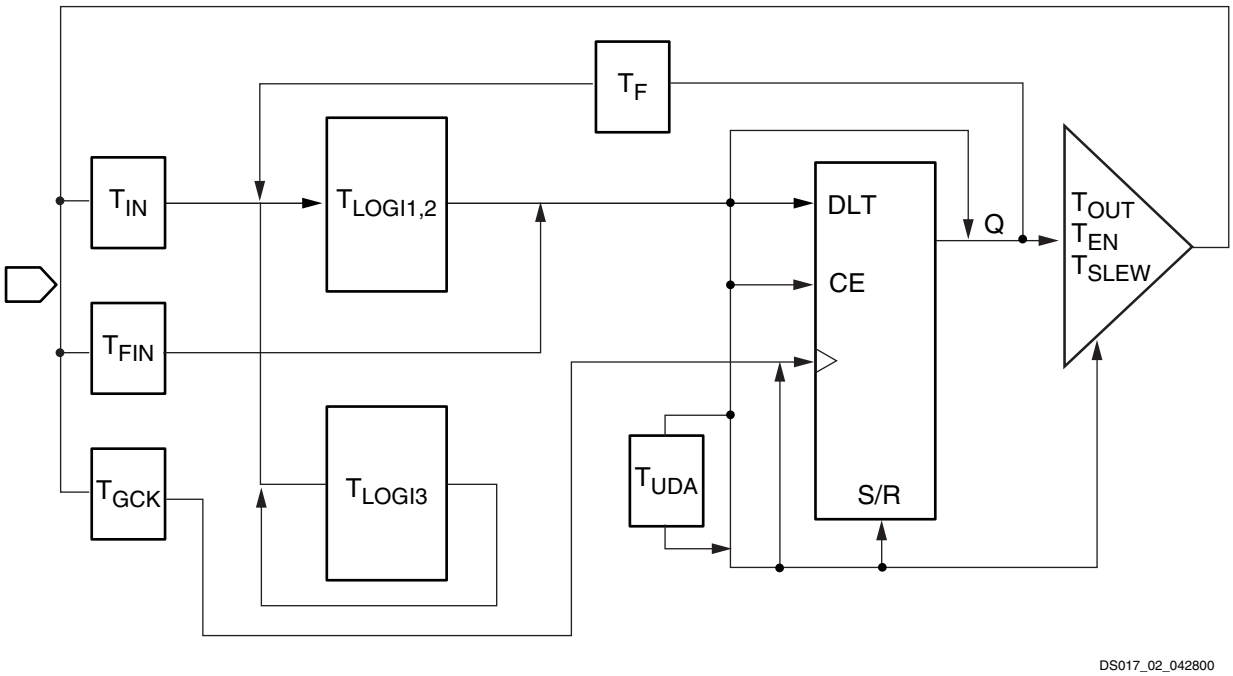


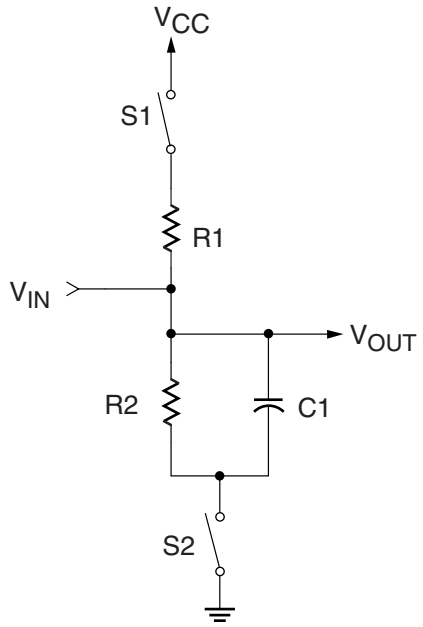
Figure 2: **XPLA3 Timing Model**

Internal Timing Parameters

Symbol	Parameter	-6		-7		-10		Unit
		Min.(1)	Max.(1)	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.3	-	1.6	-	2.2	ns
T_{FIN}	Fast Input buffer delay	-	1.8	-	2.5	-	3.1	ns
T_{GCK}	Global Clock buffer delay	-	0.8	-	1.0	-	1.3	ns
T_{OUT}	Output buffer delay	-	2.2	-	2.7	-	3.6	ns
T_{EN}	Output buffer enable/disable delay	-	4.0	-	5.0	-	5.7	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	
T_{SUI}	Register setup time	1.0	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to putput delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.5	-	2.3	-	2.1	ns
T_{RAI}	Register async. recovery	-	4.0	-	5.0	-	6.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	1.7	-	2.1	-	3.0	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	6.0	-	7.5	-	9.5	ns
T_{UDA}	Universal delay	-	1.7	-	2.2	-	2.7	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns
		Advance		**Preliminary**				

Notes:
1. Contact Xilinx for update on advance specification.

Switching Characteristics



Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

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Figure 3: **AC Load Circuit**

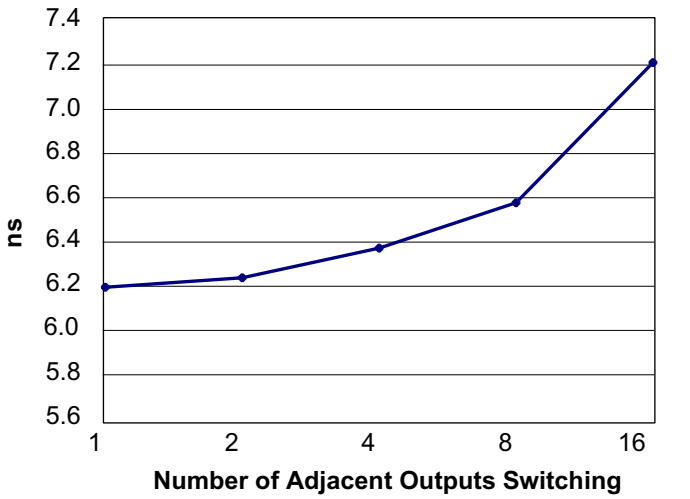

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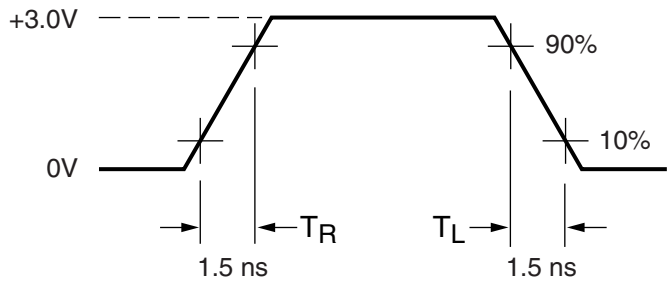
Figure 4: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

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Figure 5: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3128XL Pin Descriptions**

Function	TQ144	VQ100	CS144	BScan Order
A0	106	-	B12	440
A1 (TDO)	104 (TDO)	73 (TDO)	D11	-
A2	102	72	D12	432
A3	101	71	D13	428
A4	100	70	E10	424
A5	99	69	E11	420
A6	98	68	E12	416
A10	97	67	E13	409
A11	96	-	F10	405
A12	94	65	F12	401
A13	93	64	F13	397
A14	92	63	G10	393
A15	91	-	G11	389
B0	107	75	A13	330
B1	109	76	A12	326
B2	110	77	B11	322
B3	111	78	A11	318
B4	112	79	D10	314
B5	113	80	C10	310
B6	114	81	B10	306
B10	116	83	D9	299
B11	117	84	C9	295
B12	118	85	B9	291
B13	119	-	A9	287
B14	120	-	D8	283
B15	121	-	C8	279
C0	90	-	G13	385
C1 (TCK)	89 (TCK)	62 (TCK)	G12 (TCK)	-
C2	88	61	H13	377
C3	87	60	H12	373
C4	86	-	H11	369
C5	84	58	J13	365
C6	83	57	J12	361

Table 2: **XCR3128XL Pin Descriptions *(Continued)***

Function	TQ144	VQ100	CS144	BScan Order
C10	82	56	J11	354
C11	81	55	J10	350
C12	80	54	K13	346
C13	79	53	K12	342
C14	78	52	K11	338
C15	77	-	K10	334
CLK0/IN0	128	90	D7	-
CLK1/IN1	127	89	C7	-
CLK2/IN2	126	88	A7	-
CLK3/IN3	125	87	B7	-
D0	60	-	M8	275
D1	61	40	L8	271
D2	62	41	K8	267
D3	63	42	N9	263
D4	65	44	L9	259
D5	66	45	K9	255
D6	67	46	N10	251
D10	68	47	M10	244
D11	69	48	L10	240
D12	70	49	N11	236
D13	71	50	M11	232
D14	72	-	L11	228
D15	74	-	M12	224
E0	1	2	A1	220
E1	143	1	A2	216
E2	142	100	C3	212
E3	141	99	B3	208
E4	140	98	A3	204
E5	139	97	C4	200
E6	138	96	B4	196
E10	137	-	A4	189
E11	136	-	D5	185
E12	134	94	B5	181
E13	133	93	A5	177
E14	132	92	D6	173

Table 2: **XCR3128XL Pin Descriptions *(Continued)***

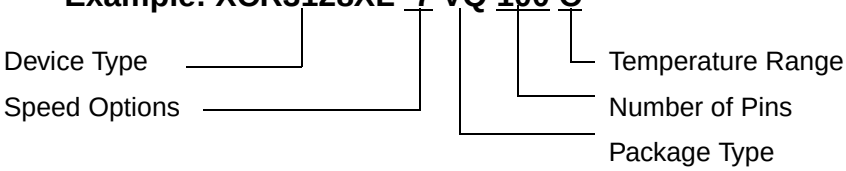
Function	TQ144	VQ100	CS144	BScan Order
E15	131	-	C6	169
F0	2	-	B1	110
F1(TDI)	4 (TDI)	4 (TDI)	D2 (TDI)	-
F2	5	5	D1	102
F3	6	6	E4	98
F4	7	7	E3	94
F5	8	8	E2	90
F6	9	9	E1	86
F10	10	10	F4	79
F11	11	-	F3	75
F12	12	-	F2	71
F13	14	12	G2	67
F14	15	13	G1	63
F15	16	14	G3	59
G0	56	-	N7	165
G1	55	37	M7	161
G2	54	36	N6	157
G3	53	35	M6	153
G4	46	33	M5	149
G5	45	32	L5	145
G6	44	31	K5	141
G10	42	30	N4	134
G11	41	29	M4	130
G12	40	28	L4	126
G13	39	27	K4	122
G14	38	-	N3	118
G15	37	-	M3	114
H0	18	-	H1	55
H1 (TMS)	20 (TMS)	15 (TMS)	H2 (TMS)	-
H2	21	16	H3	47
H3	22	17	H4	43
H4	23	-	J1	39
H5	25	19	J3	35
H6	26	20	J4	31
H10	27	21	K1	24

Table 2: **XCR3128XL Pin Descriptions *(Continued)***

Function	TQ144	VQ100	CS144	BScan Order
H11	28	22	K2	20
H12	29	23	K3	16
H13	30	24	L1	12
H14	31	25	M2	8
H15	32	-	N1	4
PORT_EN	13 (PE)	11 (PE)	F1 (PE)	-
GND	3	-	D3	-
GND	17	-	G4	-
GND	33	26	N2	-
GND	52	-	L6	-
GND	57	38	L7	-
GND	59	-	N8	-
GND	64	43	M9	-
GND	85	59	H10	-
GND	105	74	C13	-
GND	124	86	A8	-
GND	129	-	A6	-
GND	135	95	C5	-
V_{CC}	-	3	D4	-
V_{CC}	24	18	J2	-
V_{CC}	50	34	N5	-
V_{CC}	51	-	K6	-
V_{CC}	58	39	K7	-
V_{CC}	73	-	N12	-
V_{CC}	76	51	L13	-
V_{CC}	95	66	F11	-
V_{CC}	115	82	A10	-
V_{CC}	123	-	B8	-
V_{CC}	130	91	B6	-
V_{CC}	144	-	B2	-

Ordering Information

Example: XCR3128XL -7 VQ 100 C



Speed Options

-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay
-6: 6.0 ns pin-to-pin delay

Temperature Range

C = Commercial T_A = 0°C to +70°C
I = Industrial T_A = –40°C to +85°C

Packaging Options

TQ144: 144-pin Thin Quad Flat Package
CS144: 144-ball Chip Scale Package
VQ100: 100-pin Very Thin Quad Flat Package

Table 3: **XCR3128XL JTAG Pinout by Package Type**

Device XCR3128XL	(Pin Number)				
	TCK	Port Enable	TMS	TDI	TDO
144-pin TQFP	89	13	20	4	104
144-pin CS	G12	F1	H2	D2	D11
100-pin VQFP	62	11	15	4	73

Component Availability

Pins		144	144	100
Type		Plastic TQFP	Plastic BGA	Plastic VQFP
Code		TQ144	CS144	VQ100
XCR3128XL	-7	C	C	C
	-10	C,I	C,I	C,I

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
04/07/00	1.0	Initial Xilinx release.
05/03/00	1.1	Minor updates and added Boundary Scan to pinout table.