Data Sheet | June 1999 | FN3281.5

Monolithic, Quad SPST, CMOS Analog Switches

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

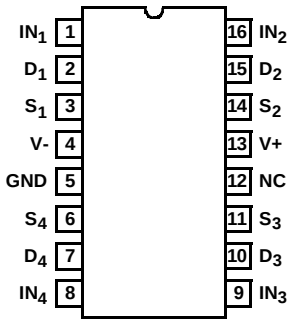
The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG441DJ	-40 to 85	16 Ld PDIP	E16.3
DG441DY	-40 to 85	16 Ld SOIC	M16.15
DG442DJ	-40 to 85	16 Ld PDIP	E16.3
DG442DY	-40 to 85	16 Ld SOIC	M16.15

Pinout

DG441, DG442
(PDIP, SOIC)
TOP VIEW



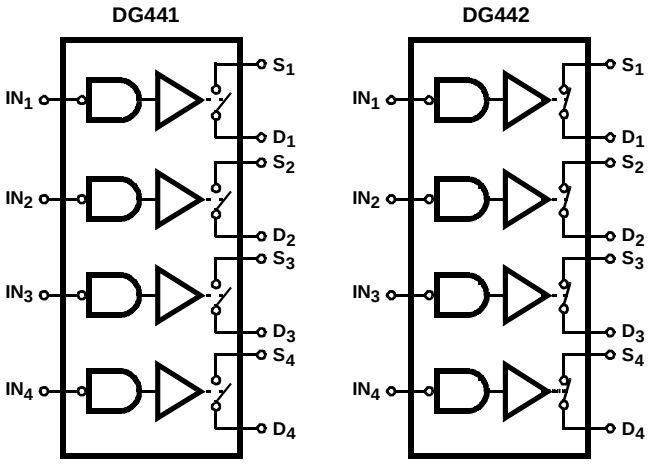
Features

- ON Resistance (Max) 85Ω
- Low Power Consumption (P_D) . . . . . <1.6mW
- Fast Switching Action
  - t_{ON} (Max) 250ns
  - t_{OFF} (Max, DG441) 120ns
- Low Charge Injection
- Upgrade from DG201A/DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Functional Diagrams

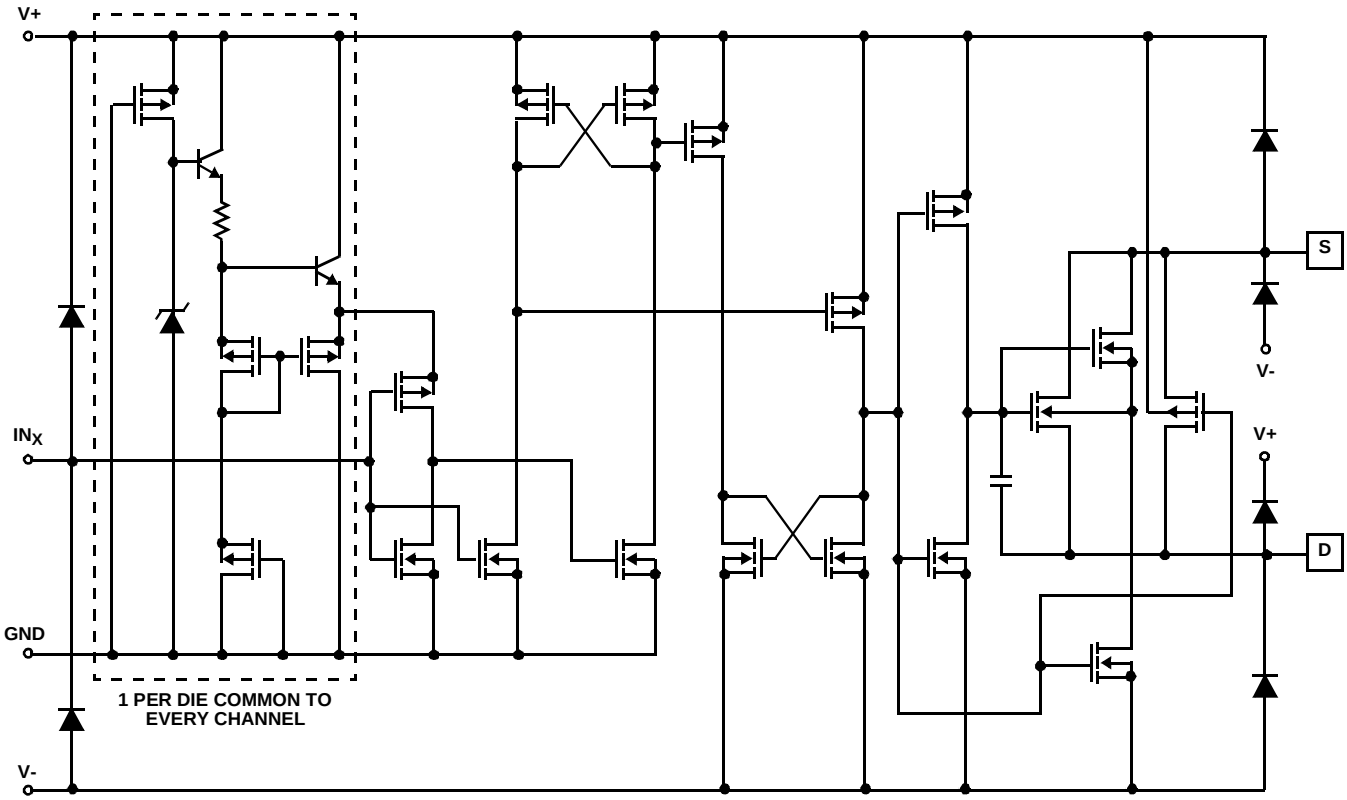


SWITCHES SHOWN FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

Schematic Diagram (One Channel)



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	NC	No Internal Connection
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

Absolute Maximum Ratings

V+ to V- 44.0V
GND to V- 25V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) . . 100mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Voltage Range . . . . . ±20V (Max)
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Plastic Packages) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S, V_D$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN	(NOTE 3) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, (Figure 1)	25	-	150	250	ns
Turn-OFF Time, t_{OFF} DG441		25	-	90	120	ns
DG442			-	110	210	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 0V, R_G = 0Ω	25	-	-1	-	pC
OFF Isolation (Figure 4)	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	60	-	dB
Crosstalk (Channel-to-Channel) (Figure 3)		25	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_{ANALOG} = 0 (Figure 5)	25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$		25	-	16	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	25	-	50	85	Ω
		85	-	-	100	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		85	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		25	-0.5	0.01	0.5	nA
		85	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D$ = ±15.5V	25	-0.5	0.08	0.5	nA
		85	-10	-	10	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{IN} = 2.4V, 0.8V, Unless Otherwise Specified

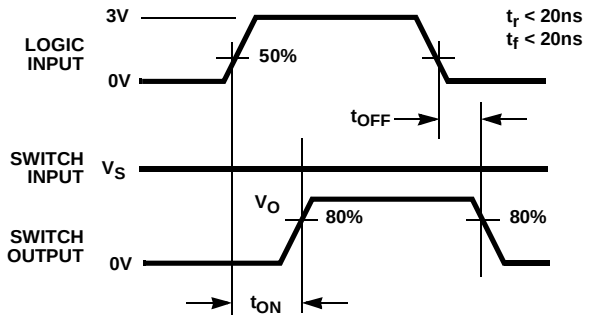
PARAMETER	TEST CONDITIONS	TEMP (^{O}C)	MIN	(NOTE 3) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V, (Figure 1)	25	-	300	450	ns
Turn-OFF Time, t_{OFF}		25	-	60	200	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 6V, R_G = 0Ω	25	-	2	-	pC
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = 10mA, V_D = 3V, 8V V+ = 10.8V	25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Full	-100	-0.0001	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

NOTES:

3. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

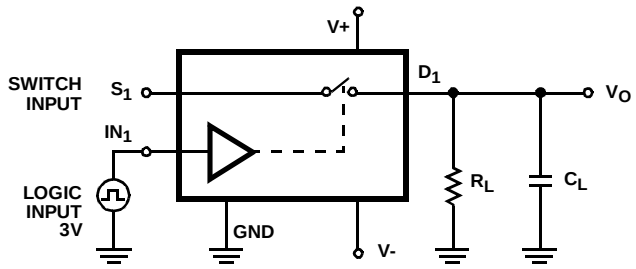
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

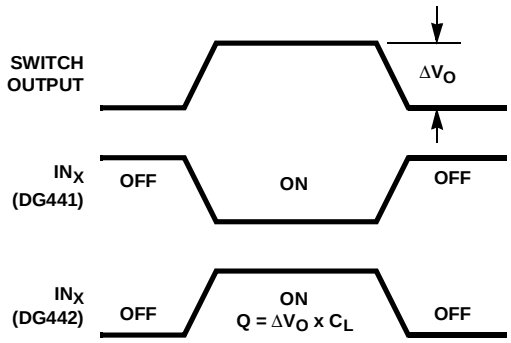


FIGURE 2A. MEASUREMENT POINTS

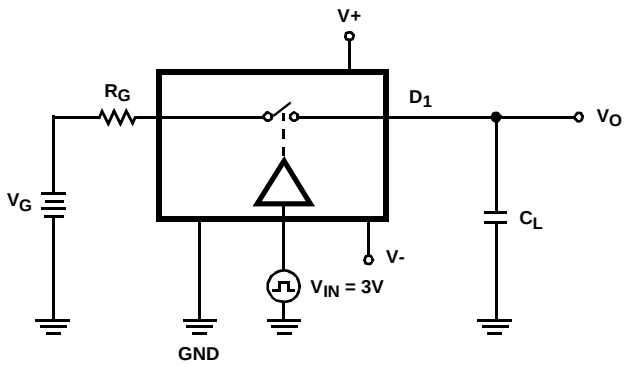


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

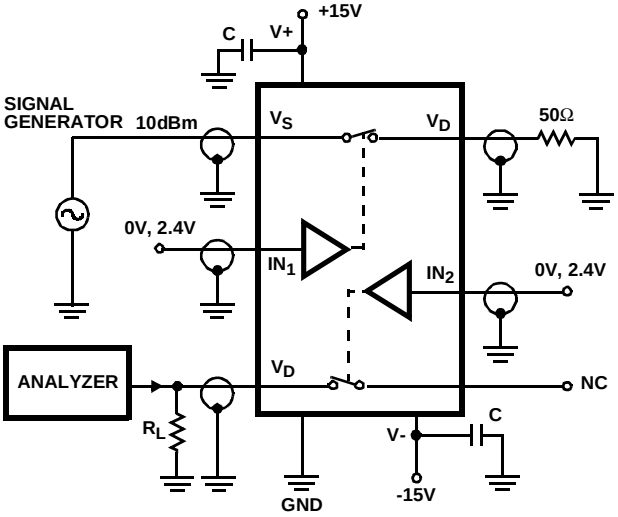


FIGURE 3. CROSSTALK TEST CIRCUIT

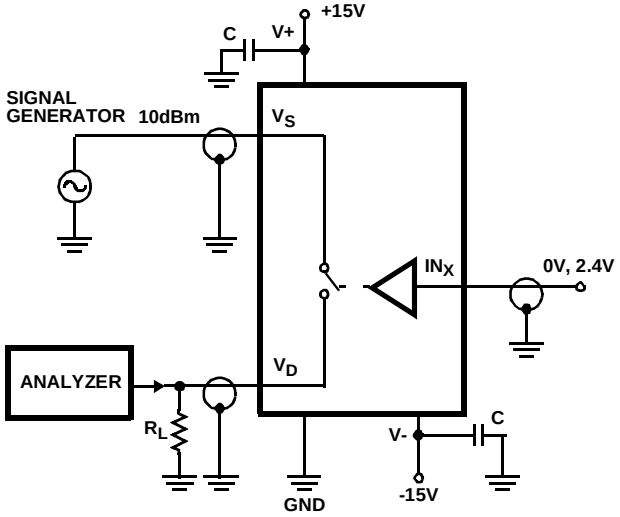


FIGURE 4. OFF ISOLATION TEST CIRCUIT

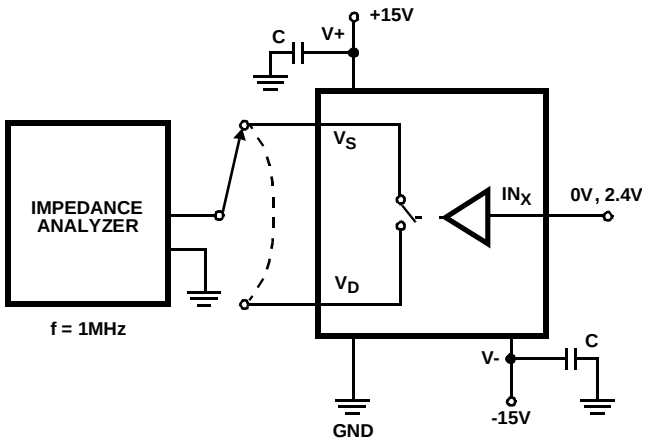
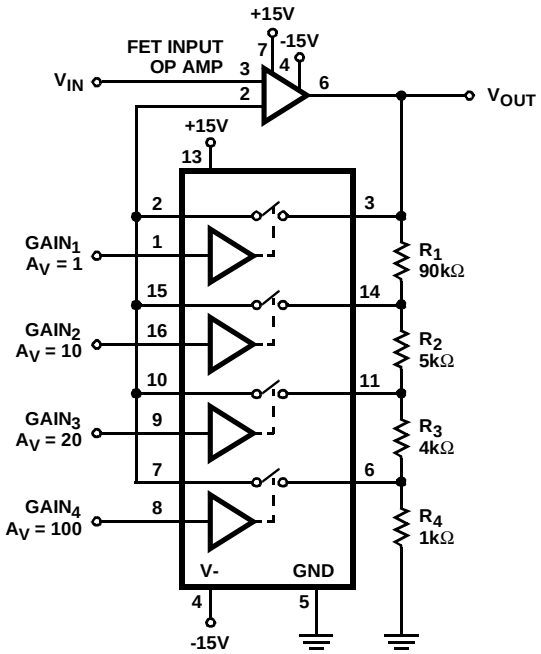


FIGURE 5. SOURCE/DRAIN CAPACITANCES TEST CIRCUIT

Application Information

GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE. OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT.



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100 \text{ with } SW_4 \text{ closed}$$

FIGURE 6. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

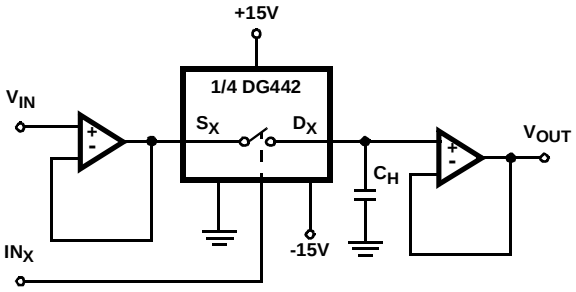


FIGURE 7. OPEN LOOP SAMPLE AND HOLD

Typical Performance Curves

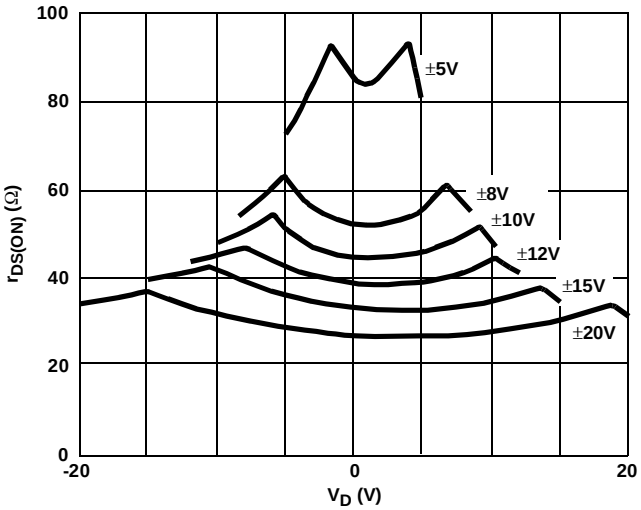


FIGURE 8. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

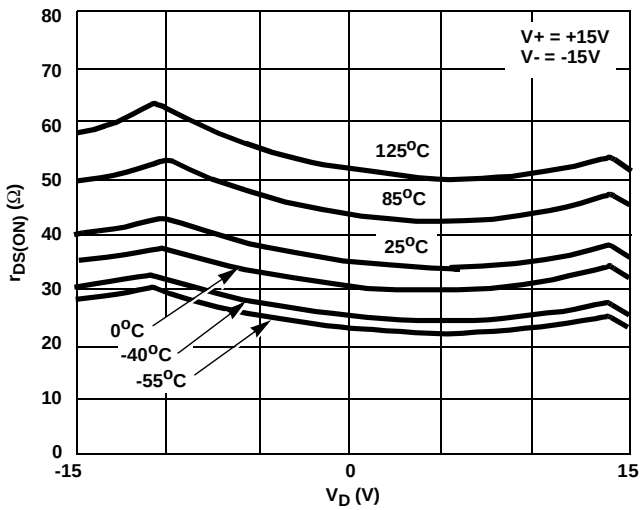


FIGURE 9. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

Typical Performance Curves (Continued)

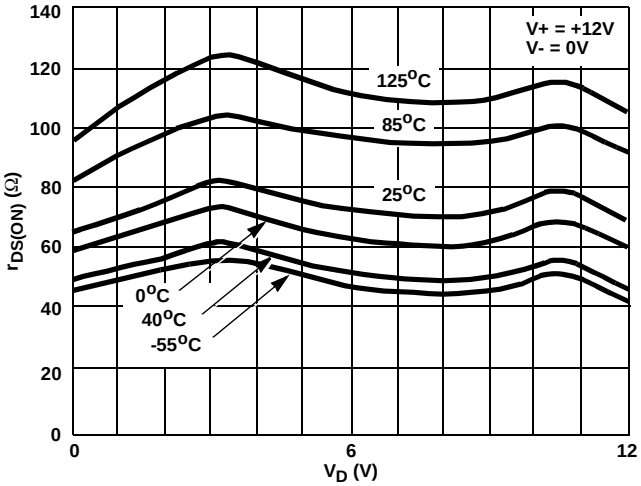


FIGURE 10. $r_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)

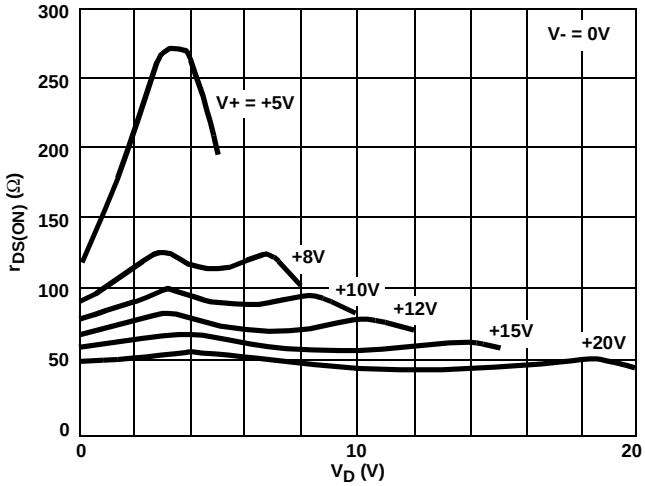


FIGURE 11. $r_{DS(ON)}$ vs V_D AND SINGLE SUPPLY VOLTAGE

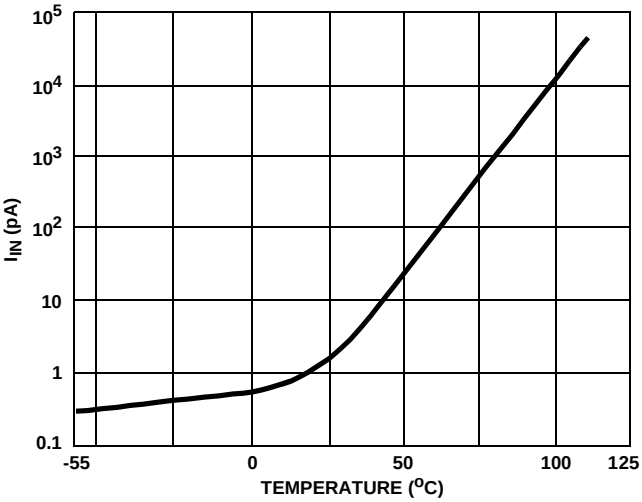


FIGURE 12. INPUT CURRENT vs TEMPERATURE

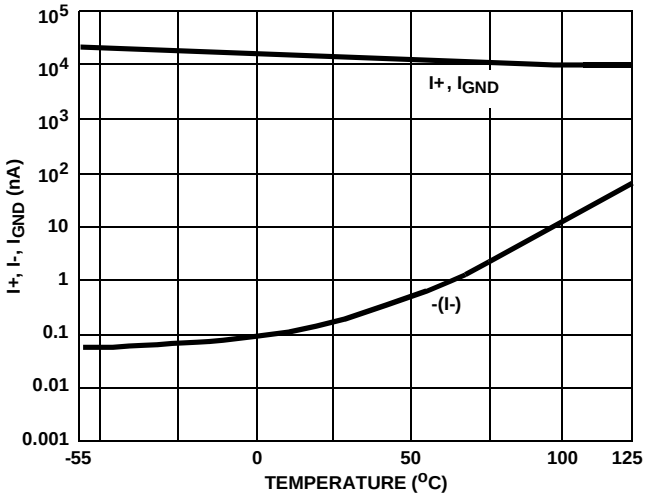


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

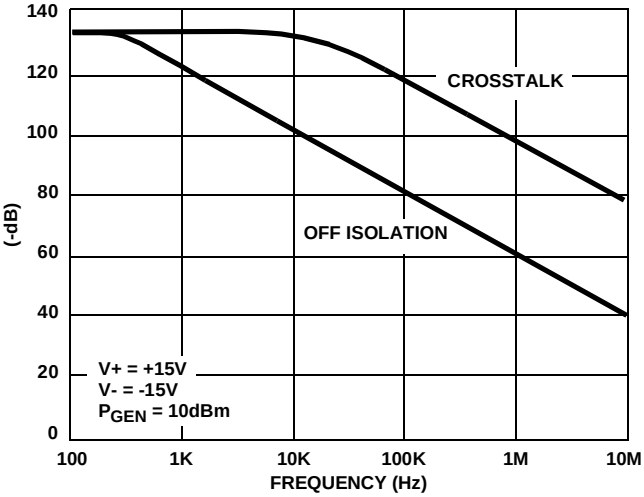


FIGURE 14. CROSSTALK AND OFF ISOLATION vs FREQUENCY

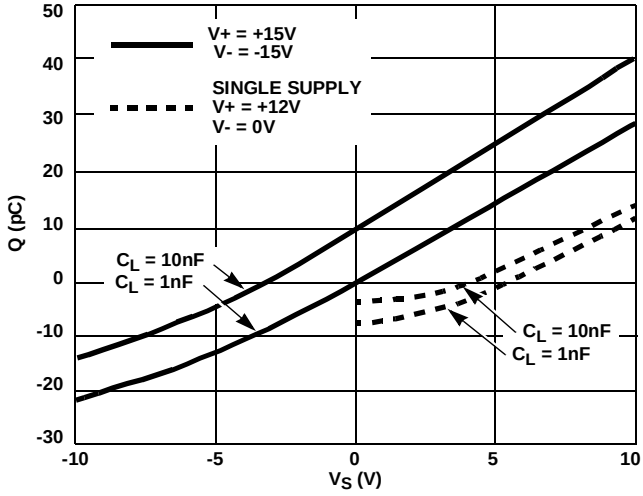


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

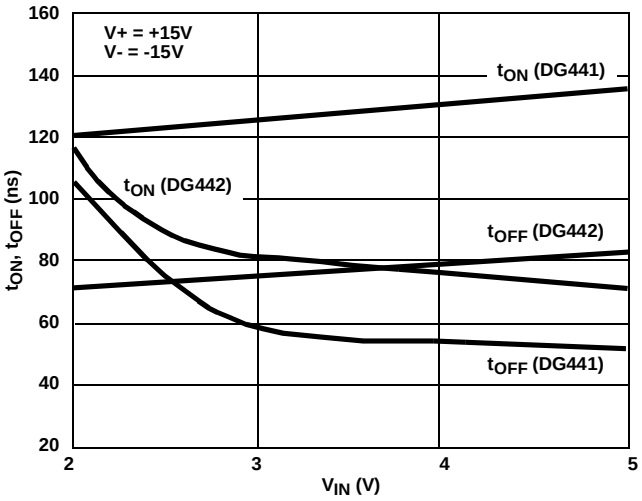


FIGURE 16. SWITCHING TIMES vs INPUT VOLTAGE

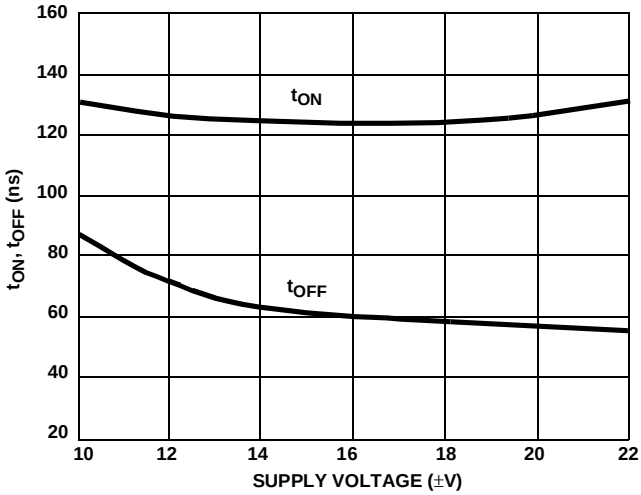


FIGURE 17. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

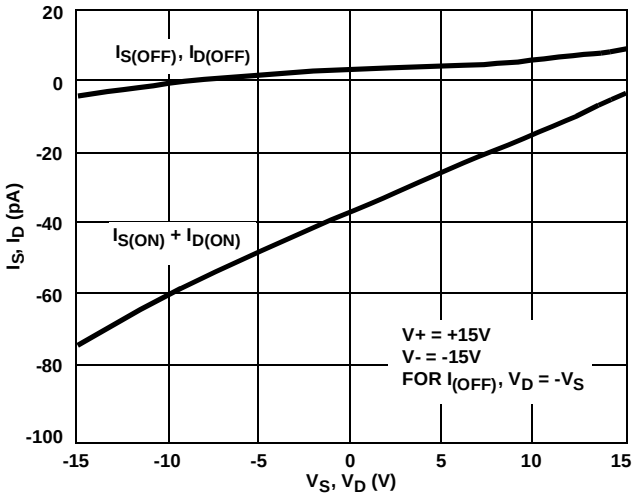


FIGURE 18. LEAKAGE CURRENT VS ANALOG VOLTAGE

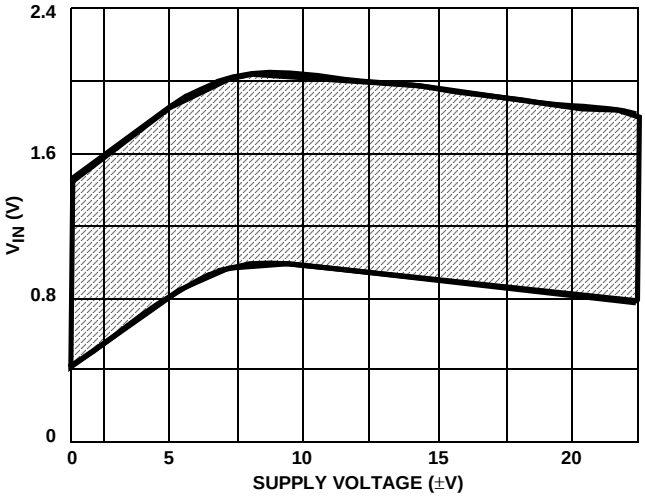


FIGURE 19. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

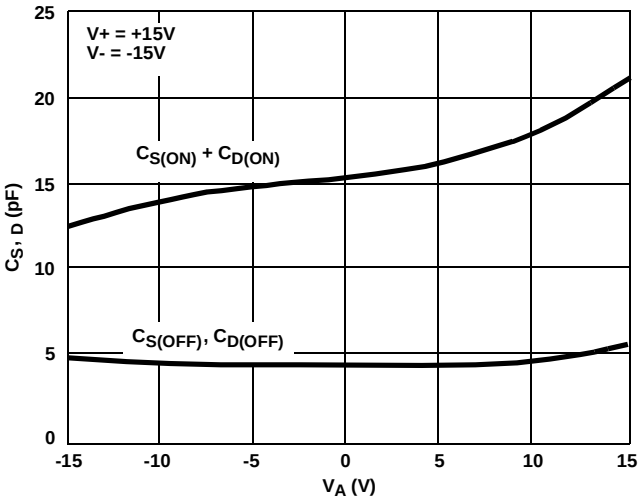


FIGURE 20. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

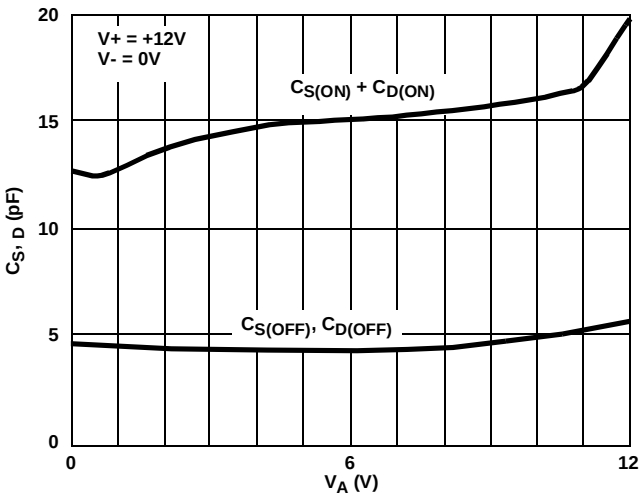


FIGURE 21. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

Typical Performance Curves (Continued)

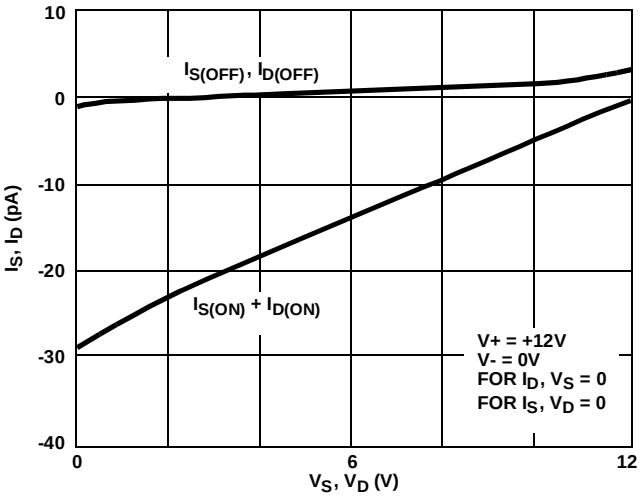


FIGURE 22. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

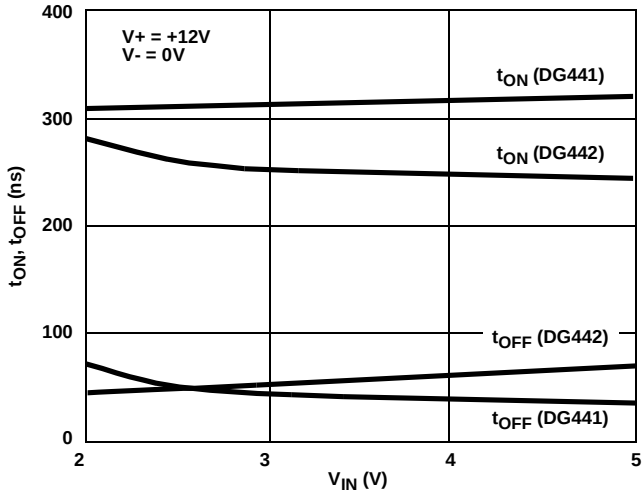


FIGURE 23. SWITCHING TIME vs INPUT VOLTAGE (SINGLE 12V SUPPLY)

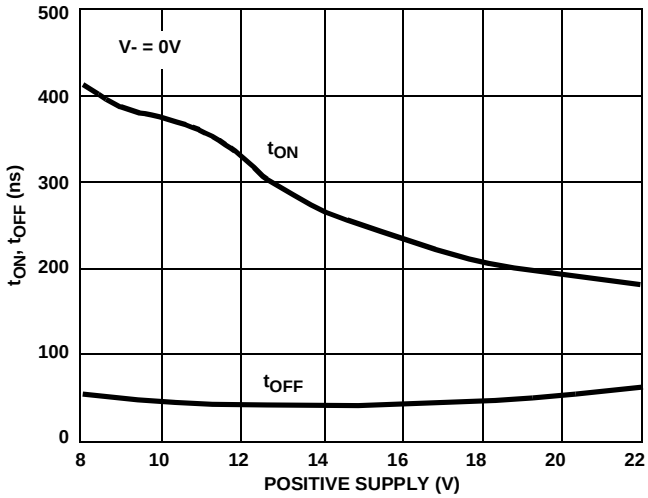


FIGURE 24. SWITCHING TIME vs SINGLE SUPPLY VOLTAGE (DG441)

Die Characteristics

DIE DIMENSIONS:

2160µm x 1760µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

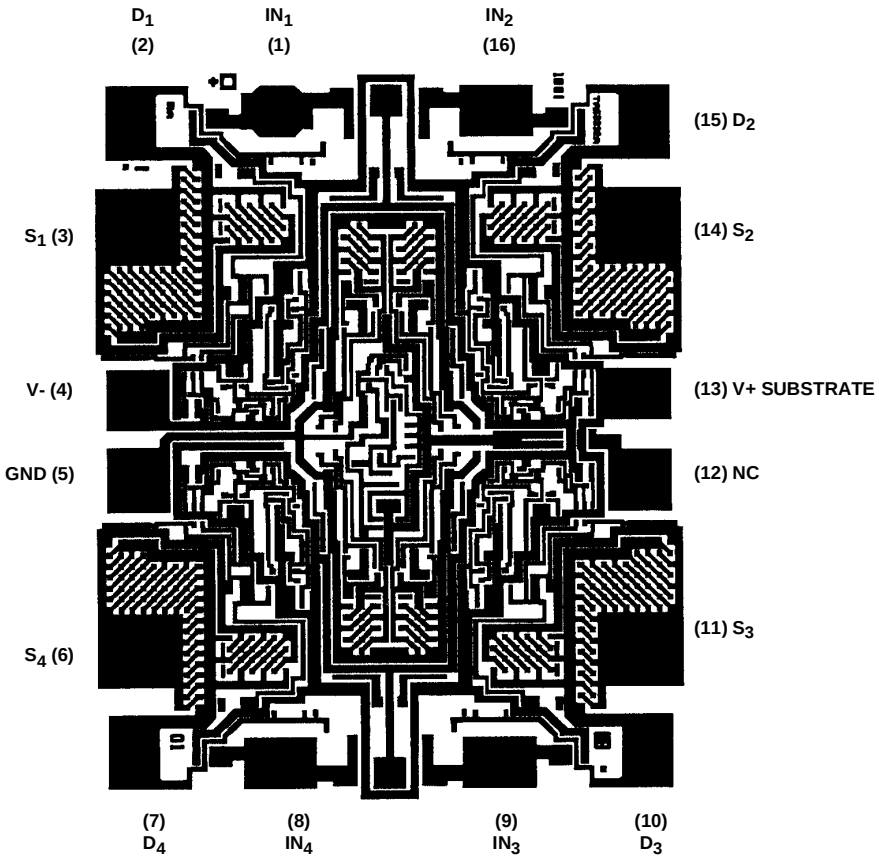
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG441, DG442



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